Amendments to the Claims

This listing of claims will replace all prior version, and listings, of claims in the application.

Listing of Claims:

1. (Original) A circuit comprising:

a parallel arrangement of segments, each segment comprising prebuffer and output stage circuitry and each segment enabled independently to achieve multiple power levels and multiple levels of pre-emphasis while maintaining a substantially constant propagation delay in a signal path of a serial link transmitter.

2. (Original) The circuit of claim 1 wherein a plurality of input signals selectively enable the parallel segments in order to balance desired amplitude and pre-emphasis needs in the transmitter signal path.

3. (Original) The circuit of claim 2 wherein the parallel segments further comprise undelayed and delayed segments to balance current steering with pre-emphasis levels in the transmitter signal path.

4. (Original) The circuit of claim 1 further comprising a bypass path in circuitry of the prebuffer stage circuitry to implement a controllable idle state in the segments.

5. (Original) The circuit of claim 4 wherein the bypass path further comprises a bypass transistor in the prebuffer stage circuitry.

6. (Original) The circuit of claim 1 further comprising tail current and resistive load elements in the prebuffer circuitry as sectioned portions for slew rate control capability.

7. (Original) The circuit of claim 1 further comprising a control element with pre-emphasis delay circuitry in the transmitter signal path to allow inversion of a last delayed bit of the pre-emphasis delay circuitry to achieve a polarity change of a pre-emphasis weight.

8. (Currently amended) A method comprising:

providing portions of a transmitter signal path as parallel segments; and

independently enabling each of the parallel segments to control output signal amplitude, wherein the parallel segments further comprise undelayed and delayed segments to balance current steering with pre-emphasis levels in the transmitter signal path.

9. (Original) The method of claim 8 wherein the step of providing further comprises providing prebuffer and output stage circuitry as the parallel segments.

10. (Original) The method of claim 8 wherein the step of independently enabling each of the parallel segments further comprises utilizing a plurality of input signals for the parallel segments that selectively enable the parallel segments in order to balance desired amplitude and pre-emphasis needs in the transmitter signal path.

11. (Cancelled)

12. (Original) The method of claim 9 further comprising providing a bypass path in circuitry of the prebuffer stage circuitry to implement a controllable idle state in the segments.

13. (Original) The method of claim 9 further comprising providing tail current and resistive load elements in the prebuffer circuitry as sectioned portions for slew rate control capability.

14. (Original) The method of claim 8 further comprising providing a control element with pre-emphasis delay circuitry in the transmitter signal path to allow inversion of a last delayed bit of the pre-emphasis delay circuitry to achieve a polarity change of a pre-emphasis weight.

15. (Original) A system comprising:

a differential input signal; and

a plurality of segments coupled in parallel for transmitting the differential input signal, wherein independent enabling of the plurality of segments provides multiple power levels and multiple levels of pre-emphasis while maintaining a substantially constant propagation delay in a signal path of the differential data signal.

16. (Original) The system of claim 15 wherein the plurality of segments further comprise a first number of segments receiving a differential data signal in an undelayed manner and a second number of segments receiving the differential data signal in a delayed manner.

17. (Original) The system of claim 15 wherein the plurality of segments each further comprise prebuffer circuitry and output stage circuitry.

18. (Original) The system of claim 17 wherein the prebuffer circuitry further comprises a bypass path to implement a controllable idle state in the segments.

19. (Original) The system of claim 18 wherein the bypass path further comprises a bypass transistor.

20. (Original) The system of claim 17 wherein the prebuffer stage circuitry further comprises tail current and resistive load elements as sectioned portions for slew rate control capability.

21. (Original) The system of claim 15 further comprising a control element with pre-emphasis delay circuitry in the signal path to allow inversion of a last delayed bit of the pre-emphasis delay circuitry.

22. (New) A method comprising:

providing portions of a transmitter signal path as parallel segments; and

independently enabling each of the parallel segments to control output signal amplitude, wherein the parallel segments further comprise undelayed and delayed segments to balance current steering with pre-emphasis levels in the transmitter signal path, further comprising providing a control element with pre-emphasis delay circuitry in the transmitter signal path to

allow inversion of a last delayed bit of the pre-emphasis delay circuitry to achieve a polarity change of a pre-emphasis weight.